Ahsanullah University of Science and Technology

Department of Electrical and Electronic Engineering

LABORATORY MANUAL

FOR

ELECTRICAL AND ELECTRONIC SESSIONAL COURSES

Student Name :

Student ID :

Course No. : EEE 2178

Course Title : Introduction to Analog and Digital Electronics Sessional

For the students of

Department of Industrial and Production Engineering

2nd Year, 1st Semester

Table of Contents

Experiment No: 01

Name of the Experiment : I-V Characteristics of diode.

Objective :

Study the I-V characteristic of diode.

Theory :

A diode is a bi-polar device that behaves as the short circuit when it is in forward bias and as an open circuit when it is in reverse bias condition.

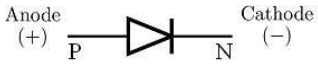


Figure 1.1 : Schematic Diagram of Diode.

Figure 1.2 : P - N Junction Diode .

There are two types of biasing condition for a diode :

1. When the diode is connected across a voltage source with positive polarity of source connected to p side of diode and negative polarity to n side, then the diode is in forward bias condition.

2. When the diode is connected across a voltage source with positive polarity of source connected to n side of diode and negative polarity to p side, then the diode is in reverse bias condition.

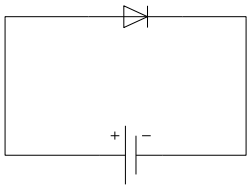


Figure 1.3 : Forward Bias connection.

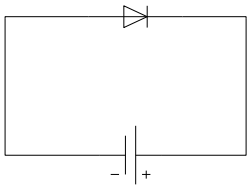


Figure 1.4 : Reverse Bias connection.

If the input voltage is varied and the current through the diode corresponds to each voltage are taken then the plot of diode current (I_d) vs diode voltage (V_D) will be follows :

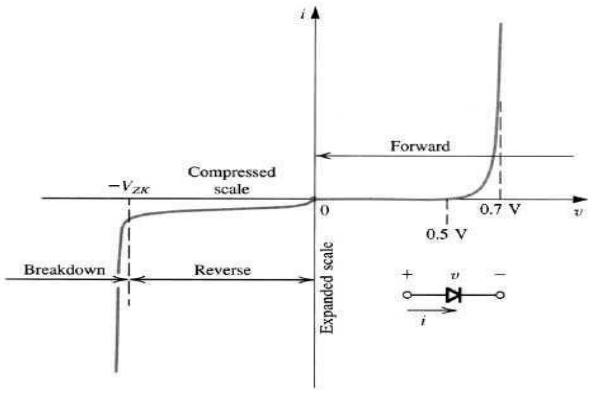


Figure 1.5 : I - V Characteristics of Diode.

At the reverse bias condition the amount of current flows through the diode is very small (at microampere range). But if the voltage continuously increases in reverse direction, at a certain value the diode will break down and huge amount of current will flow in reverse direction. This is called breakdown of diode. In laboratory the breakdown will not tested because it will damages the diode permanently.

From the characteristics curve it can be seen that, a particular forward bias voltage (V_T) is required to reach the region of upward swing. This voltage, V_T is called the cut-in voltage or threshold voltage of diode. For Si diode the typical value of threshold voltage is 0.7 volt and for Ge diode is 0.3 volt.

Equipments And Components :

Serial no.	Component Details	Specification	Quantity
1.	p-n junction diode	1N4007	1 piece
2.	Resistor	1KΩ	1 piece
3.	DC power supply		1 unit
4.	Signal generator		1 unit
5.	Trainer Board		1 unit
6.	Oscilloscope		1 unit
7.	Digital Multimeter		1 unit
8.	Chords and wire		as required

Experimental Setup :

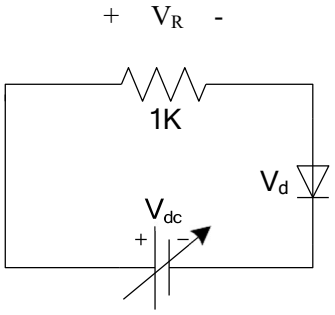


Figure 1.6 : Circuit Diagram for Obtaining Diode Obtaining Diode Forward Characteristics.

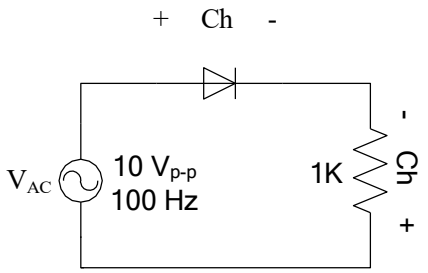


Figure 1.7 : Circuit Diagram for Characteristics From Oscilloscope.

Procedure :

1. Measure the resistance accurately using multimeter.
2. Construct the circuit as shown in figure - 1.6.
3. Vary input voltage V_{dc}. Measure V_{dc}, V_d, V_R for the given values of V_d and record data on data table. Obtain maximum value of V_d without increasing V_{dc} beyond 25 volt.
4. Calculate the values of I_d using the formula, $I_d = V_R / R$.
5. Construct the circuit as shown in figure - 1.7.
6. Ste the oscilloscope in X-Y mode. Identify zero record on oscilloscope display. Make proper connection and observe the output.
7. Repeat the step 5 and 6 by increasing the input supply frequency 5 KHz.

Data Table :

V_{dc} (volt)	V_d (volt)	V_R (volt)	$I_d = V_R / R$ (mA)

Report :

1. Draw the I - V characteristics curve of diode from the reading obtain in this experiment.
2. Calculate static resistance for I_d = 5 mA and I_d = 10 mA.
3. Determine the Q- point for the circuit in figure – 1.6, when V_{dc} = 3 volt.

Experiment No: 02

Name of the Experiment: Diode rectifier circuits.

Objective:

Study of different diode rectifier circuits.

Theory:

A rectifier converts an AC signal into a DC signal. From the characteristic curve of a diode we observe that if allows the current to flow when it is in the forward bias only. In the reverse bias it remains open. So, when an alternating voltage (signal) is applied across a diode it allows only the half cycle (positive half cycle depending on the orientation of diode in the circuit) during its forward bias condition, other half cycle will be clipped off. In the output the load will get DC signal.

Diode rectifier can be categorized in two major types. They are -

1. Half-wave rectifier.
2. Full-wave rectifier.

Half - Wave Rectifier: Half-wave rectifier can be built by using a single diode. The circuit diagram and the wave shapes of the input and output voltage of half wave rectifier are shown bellow (figure 2.1) -

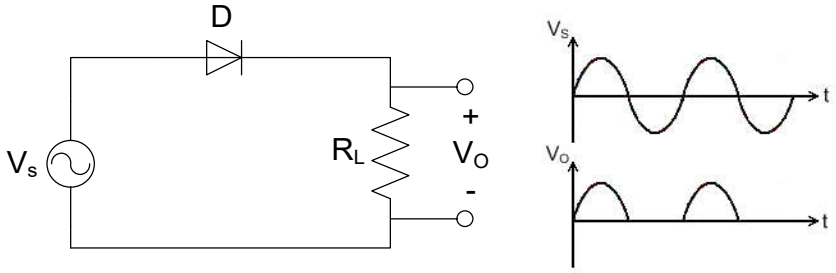


Figure 2.1: Half Wave Rectifier.

The major disadvantages of half wave rectifier are -

- In this circuit the load receives approximately half of input power.
- Average DC voltage is low.
- Due to the presence of ripple output voltage is not smooth one.

Full Wave Rectifier: in the full-wave rectifier both the half cycle is present in the output. Two circuits are used as full-wave rectifier are shown bellow -

a) Full-wave rectifier using center-tapped transformer.
b) Full-wave bridge rectifier.

Full-wave rectifier using center-tapped transformer: two diodes will be connected to the ends of the transformer and the load will be between the diode and center tap. The circuit diagram and the wave shapes are shown in bellow (figure 2.2) -

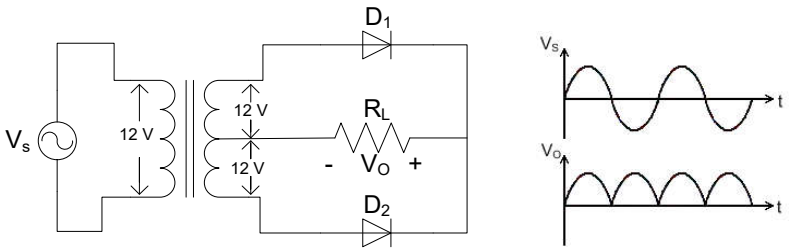


Figure 2.2: Full Wave Rectifier Using Center Tapped Transformer.

Full-wave rectifier using center-tapped transformer circuit has some advantages over full-wave rectifier. Those are -

- Wastage of power is less.
- Average DC output increase significantly.
- Wave shape becomes smoother.

The disadvantages of full-wave rectifier using center-tapped transformer are -

- Require more space and becomes bulky because of the transformer.
- Not cost effective (for using transformer).

Full-wave bridge rectifier: a bridge rectifier overcomes all the disadvantages of described above. Here four diodes will be connected as bridge connection. The circuit diagram and the wave shapes are shown in bellow (figure 2.3) -

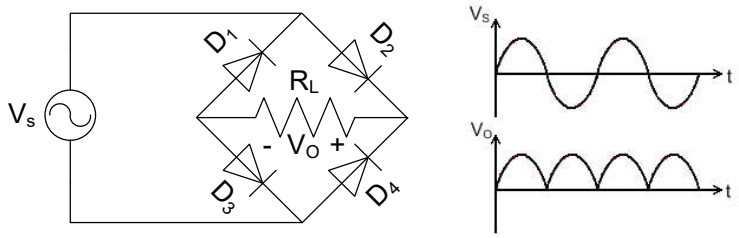


Figure 2.3: Full Wave Bridge Rectifier.

This rectifier however cannot produce a smooth DC voltage. It produces some ripple in the output. This ripple can be reducing by using filter capacitor across the load.

Equipments And Components:

Serial no.	Component Details	Specification	Quantity
1.	p-n junction diode	1N4007	4 piece
2.	Resistor	10KΩ	1 piece
3.	Capacitor	0.22µF, 10µF	1 piece each
4.	Signal generator		1 unit
5.	Trainer Board		1 unit
6.	Oscilloscope		1 unit
7.	Digital Multimeter		1 unit
8.	Chords and wire		as required

Experimental Setup:

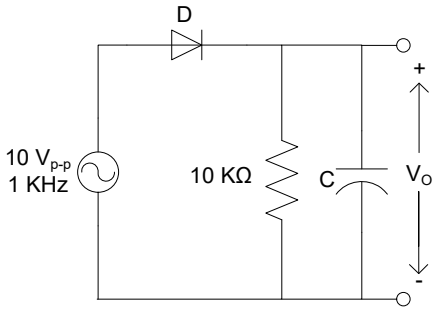


Figure 2.4 : Experimental Circuit 1.

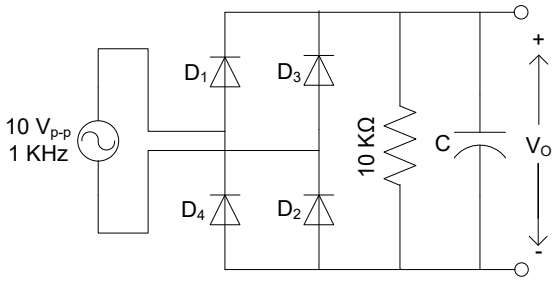


Figure 2.5 : Experimental Circuit 2.

Procedure:

1. Connect the circuit in breadboard as shown in figure 2.4 without capacitor.
2. Observe the output and input voltages in the oscilloscope and draw them.
3. Connect the 0.22µF capacitor and repeat step 2.
4. Connect the 10µF capacitor and repeat step 2. How does the output wave-shape differ from that in step 3?
5. Vary the frequency from 10 KHz to 100 Hz. What effects do you observe when frequency is changed?
6. Connect the circuit breadboard as shown in figure 2.5 without capacitor.
7. Observe the output and input voltages in the oscilloscope and draw them.
8. Connect the 0.22µF capacitor and repeat step 7.
9. Connect the 10µF capacitor and repeat step 7. How does the output wave-shape differ from that in step 8?
10. Vary the frequency from 10 KHz to 100 Hz. What effects do you observe when frequency is changed?

Report:

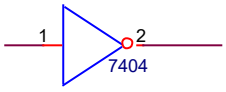
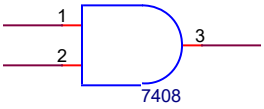
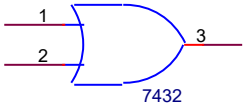
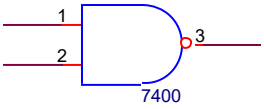
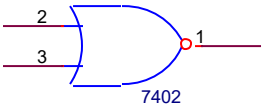
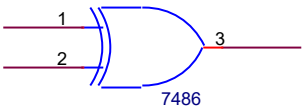
1. Write the answers that were asked during the working procedure.
2. Draw the input wave, output wave (without and with capacitor) for both the circuits.
3. What is the effect in output for changing input signal frequency for both the circuits (without and with capacitor)?
4. What is the function of capacitor in the both circuits? Why a capacitor of higher value is preferable?

Experiment: 03
Experiment name: Introduction to different digital ICs.

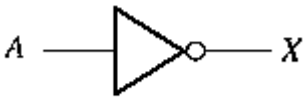
Introduction:

In this experiment you will be introduced to different digital ICs that will be used in this digital lab to perform different functions and also the function of each IC. You are asked to memorize the followings associated with each IC.

1. IC number
2. IC name
3. Total number of pins
4. V_{cc} pin number
5. Ground pin number

IC number	IC name	Schematic view
7404	NOT/INVERTER	
7408	AND	
7432	OR	
7400	NAND	
7402	NOR	
7486	XOR	

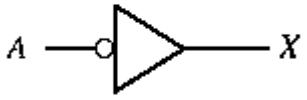
The INVERTER/NOT Gate



A	X
0	1
1	0

$X = \overline{A}$

Boolean expression



Distinctive shape symbols

Truth table

0 = LOW
1 = HIGH

The output of an inverter is always the complement (opposite) of the input.

The AND Gate

Distinctive shape symbol

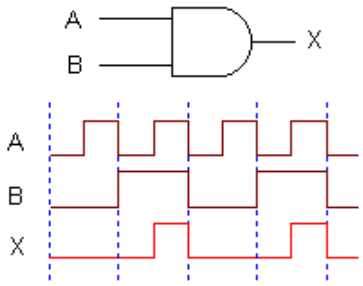
$X = AB$

Boolean expression

B	A	X
0	0	0
0	1	0
1	0	0
1	1	1

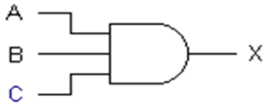
Truth table

0 = LOW
1 = HIGH



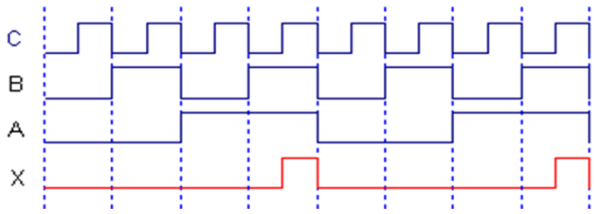
Pulsed Waveforms

The output of an AND gate is HIGH only when all inputs are HIGH.



X = ABC

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



3 Input AND Gate

The OR Gate

Distinctive shape symbol

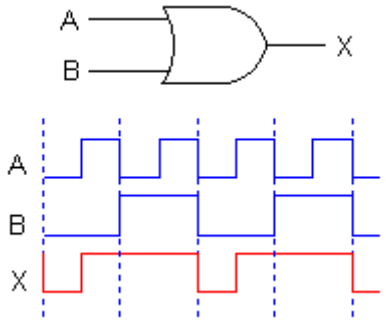
X = A + B

Boolean expression

B	A	X
0	0	0
0	1	1
1	0	1
1	1	1

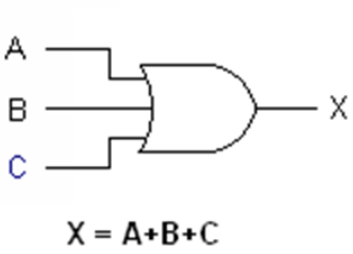
Truth table

0 = LOW
1 = HIGH



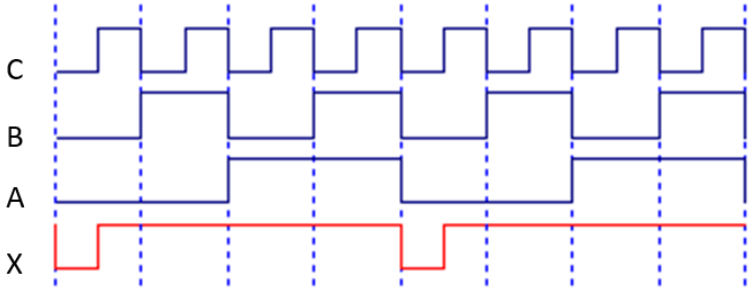
Pulsed Waveforms

The output of an OR gate is HIGH whenever one or more inputs are HIGH.



X = A+B+C

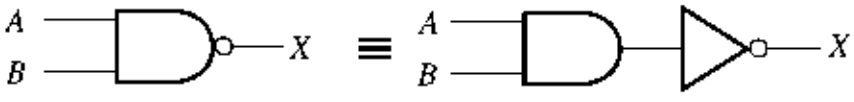
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



3 Input OR Gate

The NAND Gate

Distinctive shape symbol



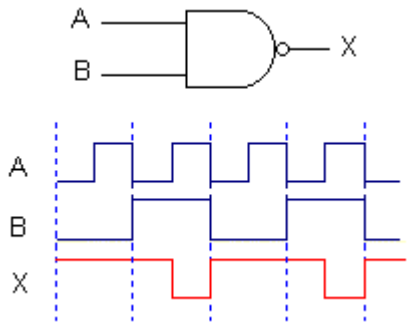
B	A	X
0	0	1
0	1	1
1	0	1
1	1	0

Truth table

0 = LOW
1 = HIGH

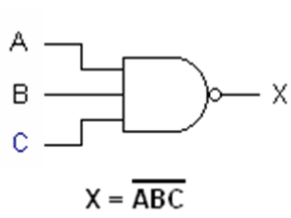
$X = \overline{AB}$

Boolean expression

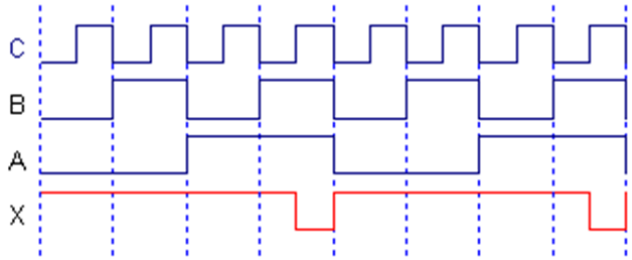


Pulsed Waveforms

The output of a NAND gate is HIGH whenever one or more inputs are LOW.

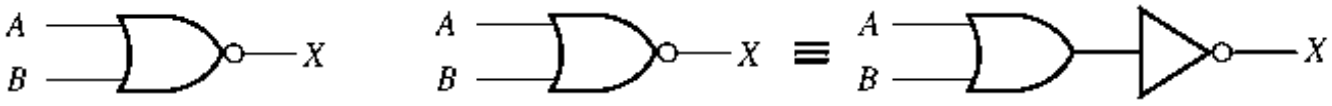


A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



3 Input NAND Gate

The NOR Gate



Distinctive shape symbol

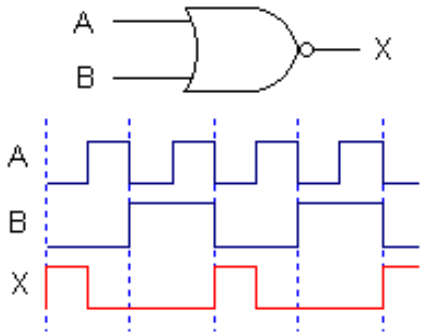
B	A	X
0	0	1
0	1	0
1	0	0
1	1	0

Truth table

0 = LOW
1 = HIGH

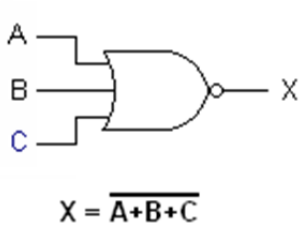
$X = \overline{A + B}$

Boolean expression



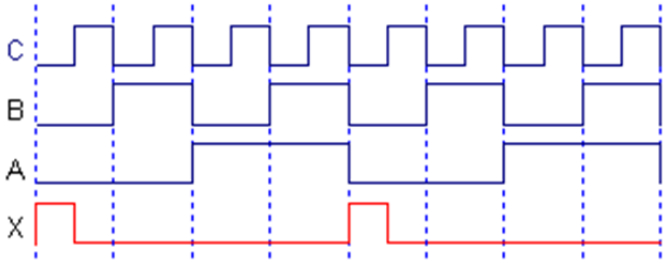
Pulsed Waveforms

The output of a NOR gate is LOW whenever one or more inputs are HIGH.



$X = \overline{A+B+C}$

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



3 Input NOR Gate

Exclusive-OR Gate

Distinctive shape symbol

B	A	X
0	0	0
0	1	1
1	0	1
1	1	0

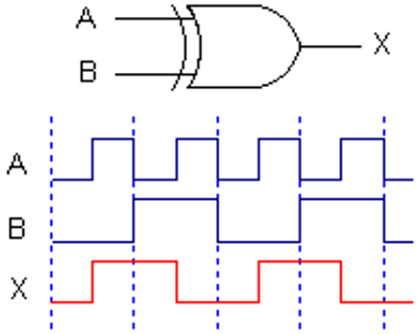
Truth table

0 = LOW
1 = HIGH

$X = A \oplus B$

Boolean expression

The output of an XOR gate is HIGH whenever the two inputs are different.



Pulsed Waveforms

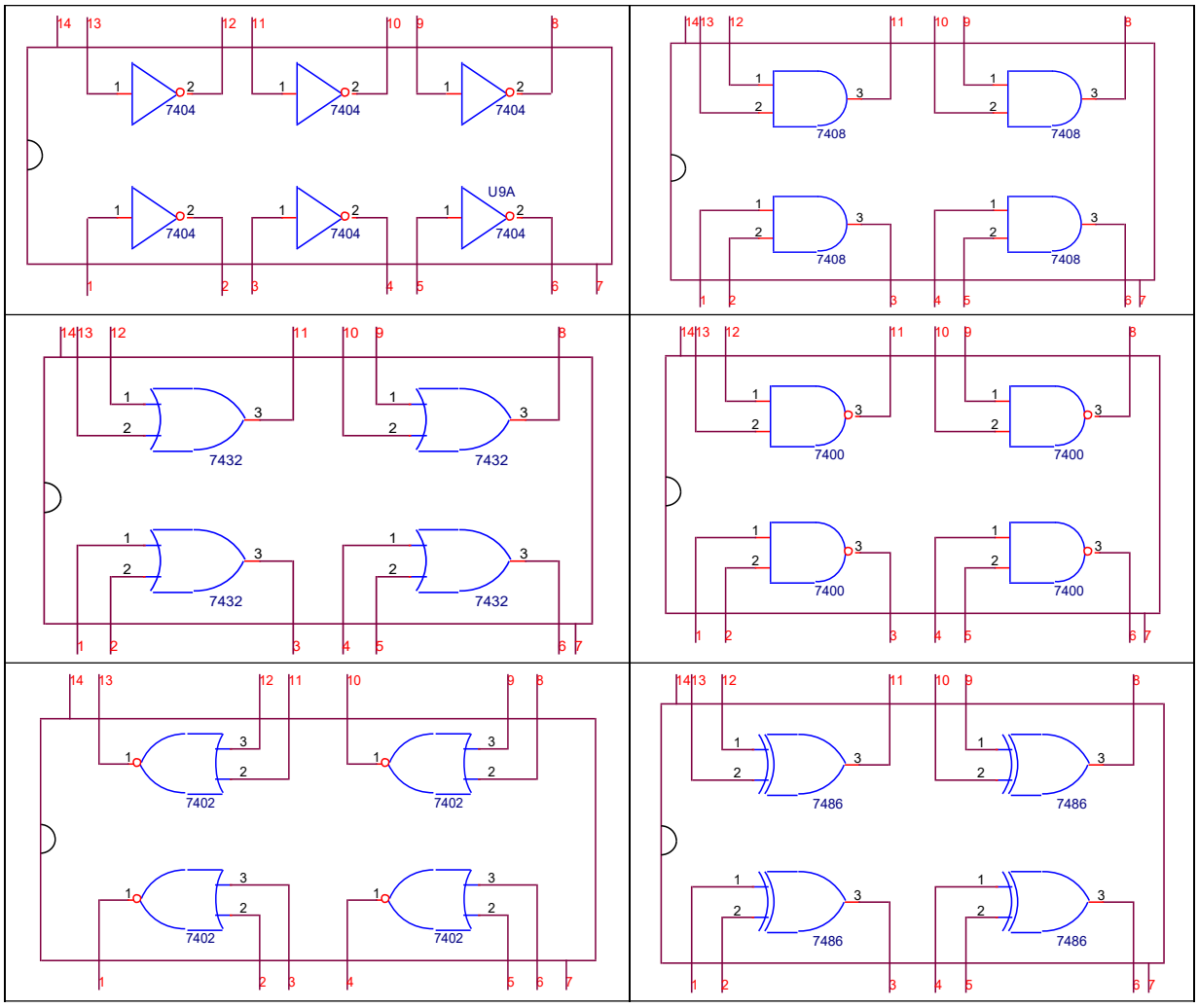
Equipment:

1. Trainer Board
2. IC 7400,7402,7404,7408,7432,7486
3. Microprocessor Data handbook

Procedure:

1. Take any of the following ICs. From microprocessor data handbook find the name of the IC, total number of pins that it has, V_{cc} pin and ground pin.

IC Number	**IC name**	**Total number of pin**	**V_{cc} pin no.**	**Ground pin no.**
7400	NAND	14	14	7
7402	NOR	14	14	7
7404	NOT	14	14	7
7408	AND	14	14	7
7432	OR	14	14	7
7486	XOR	14	14	7



2. Note the number of gates each IC has from the handbook.
3. Now fill up the following table:

Input A	**Input B**	**7400 NOT** $Y = \overline{A}$	**7432 OR** $Y = A + B$	**7402 NOR** $Y = \overline{A + B}$	**7486 XOR** $Y = A \oplus B$	**7408 AND** $Y = AB$	**7400 NAND** $Y = \overline{AB}$
0	0						
0	1						
1	0						
1	1						

4. Now verify the observed output with the desired output for different combination of inputs.
5. Repeat step 1 to 4 for different ICs.

Report:

1. How can you make a three input AND/OR/XOR gate with a two input AND/OR/XOR gate?
2. Is it possible to make a three input NAND/NOR gate with a two input NAND/NOR gate? Justify your answer.

Experiment: 04
Experiment name: Introduction to Combinational logic

Introduction:
Adders and sub tractors are the basic operational units of simple digital arithmetic operations. In this experiment, the students will construct the basic adder and sub tractor circuit with common logic gates and test their operability. Then in the last job, they will cascade adder ICs to get higher bit adders.

Binary Adder
Among the basic functions encountered are the various arithmetic operations. The most basic arithmetic operation, is the addition of two binary digits. This simple addition consists of four possible elementary operations, namely, 0 + 0 = 0, 0 + 1 = 1, 1 + 0 = 1, and 1 + 1 = 10. The first three operations produce a sum whose length is one digit, but when both augend and addend bits are equal to 1, the binary sum consists of two digits. The higher significant bit of this result is called a *carry.* When the augend and addend numbers contain more significant digits, the carry obtained from the addition of two bits is added to the next higher-order pair of significant bits. A combinational circuit that performs the addition of two bits is called a *half-adder.* One that performs the addition of three bits (two significant bits and a previous carry) is *full-adder.*

Half Adder
From the basic understanding of a half-adder, we find that the circuit needs two binary inputs and two binary outputs. The input variables designate the augend and addend bits; the output variables produce the sum and carry. It is necessary to specify two output variables because the result may consist of two binary digits. We arbitrarily assign symbols *x* and *y* to the two inputs and S (for sum) and C (for carry) to the outputs.
Now that we have established the number and names of the input and output variables, we are ready to formulate a truth table to identify exactly the function of the half-adder. This truth table is

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

The carry output is 0 unless both inputs are 1. The S output represents the least significant bit of the sum.
The simplified Boolean functions for the two outputs can be obtained directly from the truth table. The simplified sum of products expressions are

$$S = x'y + xy' = x \oplus y$$

$$C = xy$$

The logic diagram for this implementation is shown below

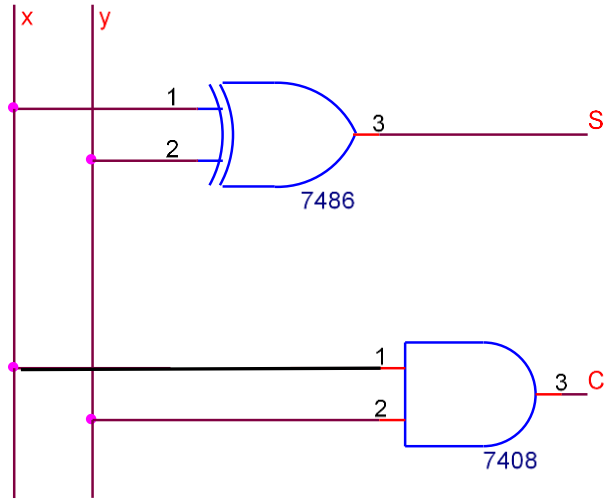


Fig 4.1. Half-adder

Full Adder

A full-adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. Two of the input variables, denoted by *x* and *y,* represent the two significant bits to be added. The third input, z, represents the carry from the previous lower significant position. Two outputs are necessary because the arithmetic sum of three binary digits ranges in value from 0 to 3, and binary 2 or 3 needs two digits. The two outputs are designated by the symbols S for sum and C for carry. The binary variable S gives the value of the least significant bit of the sum. The binary variable Cr gives the output carry. The truth table of the full-adder is

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

The eight rows under the input variables designate all possible combinations of 1's and 0's that these variables may have. The 1's and 0's for the output variables are determined from the arithmetic sum of the input bits. When all input bits are 0's, the output is 0. The S output is equal to 1 when only one input is equal to 1 or when all three inputs are equal to 1. The C output has a carry of 1 if two or three inputs are equal to 1. Physically, the binary signals of the input wires are considered binary digits added arithmetically to form a two-digit sum at the output wires. On the other hand, the same binary values are considered variables of Boolean functions when expressed in the truth table or when the circuit is implemented with logic gates. It is important to realize that two different interpretations are given to the values of the bits encountered in this circuit. The input-output logical relationship of the full-adder circuit may be expressed in two

Boolean functions, one for each output variable. This implementation uses the following Boolean expressions:

$$S = x'y'z + x'yz' + xy'z' + xyz = z'(x'y + xy') + z(x'y' + xy) = z'(x \oplus y) + z(x \oplus y)' = x \oplus y \oplus z$$
$$C = x'yz + xy'z + xyz' + xyz = x(y'z + yz') + yz(x + x') = x(y \oplus z) + yz$$

The logic diagram for the full-adder implemented in sum of products is shown in Fig. 2.2

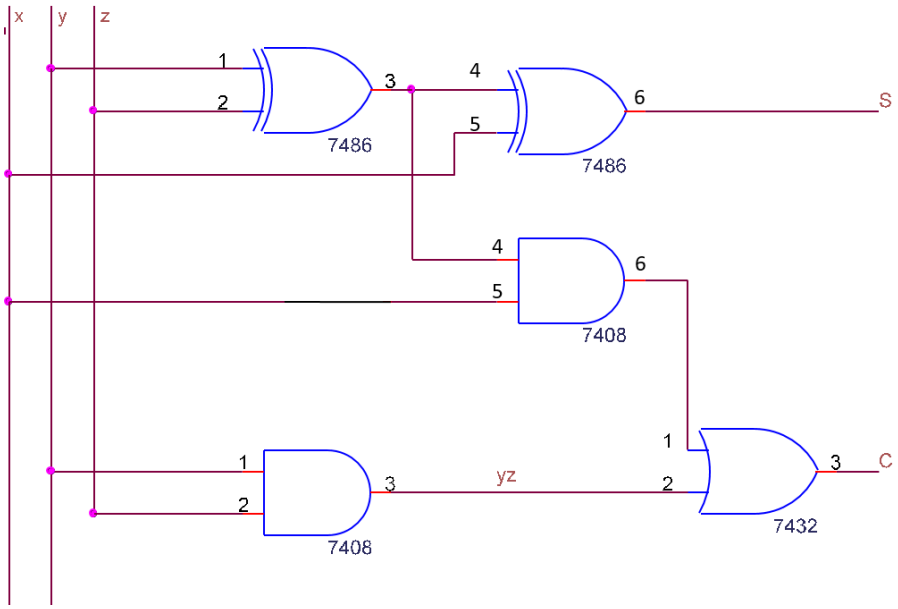


Fig 4.2. Full-adder

Half Subtractor

A half-subtractor is a combinational circuit that subtracts two bits and produces their difference. It also has an output to specify if a 1 has been borrowed. Designate the minuend bit by *X* and the subtrahend bit by *y.* To perform *x* - *y,* we have to check the relative magnitudes of *x* and *y.* If *x* '3 *y,* we have three possibilities: 0 - 0 = 0,
1 - 0 = 1, and 1 - 1 = O. The result is called the *difference bit.* If *x* < *y,* we have 0 - 1, and it is necessary to borrow a 1 from the next higher stage. The 1 borrowed from the next higher stage adds 2 to the minuend bit, just as in the decimal system a borrow adds 10 to a minuend digit. With the minuend equal to 2, the difference becomes
2 - 1 = 1. The half-subtractor needs two outputs. One output generates the difference and will be designated by the symbol *D.* The second output, designated *B* for borrow, generates the binary signal that informs the next stage that a 1 has been borrowed.
The truth table for the input-output relationships of a half-subtractor can now be derived as follows:

x	y	B	D
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

The Boolean functions for the two outputs of the half-subtractor are derived directly from the truth table:

$$D = x'y + xy' = x \oplus y$$

$$B = x'y$$

It is interesting to note that the logic for D is exactly the same as the logic for output S in the half-adder.

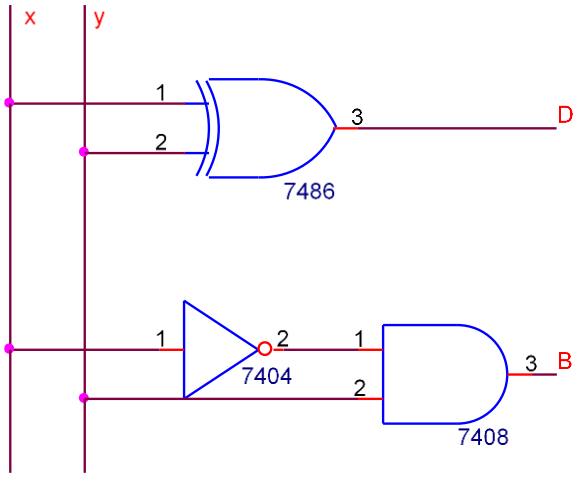


Fig 4.3. Half-subtractor

Full Subtractor

A full-subtractor is a combinational circuit that performs a subtraction between two bits, taking into account that a 1 may have been borrowed by a lower significant stage. This circuit has three inputs and two outputs. The three inputs, *x, y,* and z, denote the minuend, subtrahend, and previous borrow, respectively. The two outputs, *D* and *B,* represent the difference and output borrow, respectively. The truth table for the circuit is

x	y	z	B	D
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$D = x'y'z + x'yz' + xy'z' + xyz = x'(y'z + yz') + x(y'z' + yz) = x'(y \oplus z) + x(y \oplus z)' = x \oplus y \oplus z$$

$$B = x'y'z + x'yz' + x'yz + xyz = x'(y'z + yz') + yz(x' + x) = x'(y \oplus z) + yz$$

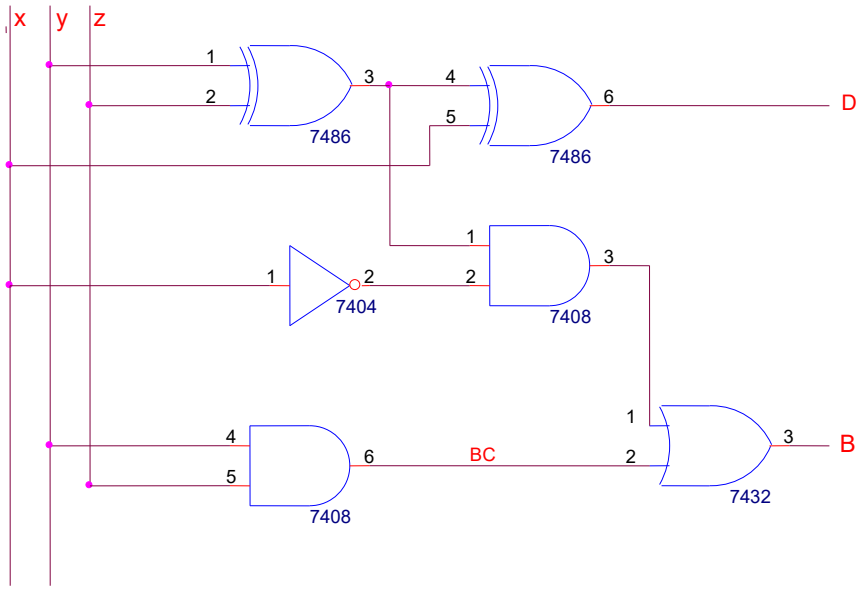


Fig 4.4. Full-subtractor

Caution:

1. Remember to properly identify the pin numbers so that no accidents occur.
2. Properly bias the ICs with appropriate pins.

Equipment:

1. Trainer Board
2. IC 7400,7402,7404,7408,7432,7486
3. Microprocessor Data handbook

Procedure:

1. Fill up the truth table for a half adder
2. Verify the Boolean function for a half adder.
3. Construct the logic diagram from the Boolean functions.
4. Select the ICs from the equipment list.
5. Implement the output logic.
6. Repeat the whole procedure for half a subtractor.
7. Fill up the truth table for a full adder.
8. Verify the Boolean function for a full adder.
9. Construct the logic diagram from the Boolean functions.
10. Select the ICs from the equipment list.
11. Implement the output logic.
12. Repeat the whole procedure for a full sub tractor.

Report

1. Design a full adder using two half adder block and basic gates.